Analysis and Implementation of Hybrid FIR Architecture in Speech Processor

Mr. Shruti Timande
Department of WCC, T.G.P.C.E.T Nagpur India
shruti.wcc.tgp@gmail.com

Article History

Article Submission
19 February 2018
Revised Submission
12 April 2018
Article Accepted
13 May 2018
Article Published
30 June 2018

Abstract

Hearing aid is an electronic gadget precisely used into the internal ear which reestablishes halfway hearing to smooth hearing. The discourse processor of CI parts the sound-related sign into groups of various frequencies and changes over them into appropriate codes for animating the cathodes in cochlea of ear. The cathode actuates sound-related nerve filaments to give hearing sensation. The expense of the CI alone goes to around 100,000 US dollars. For the efficient less well-to-do individuals with hearing sickness, it might be too exorbitant to even consider affording for this hardware to recoup from the conference misfortune. It gets important to cut down the expense. The cost decrease might be accomplished with diminished region, low force and rapid activity of the CI. This goal intuited both the simple and the computerized based CI originators to inquire about their techniques to give individuals less expensive and profoundly understandable CI. The primary objective of this paper is to develop reconfigurable DSP architectures for the filter banks in speech processor of CI with the following features like minimized area of the filter, reduced power consumption of the speech processor and enhanced presentation of the filter. This paper involves the design and hardware implementation of narrow band pass FIR filter for speech processor of CI using the Xilinx System Generator (XSG) tool on Virtex 7 FPGA.

Keywords: *speech processing, FIR, filter-bank design, signal processing, filter transfer functions*

I. Introduction

The architecture for these filters was designed using parallel filter and travelling wave filter cascade [1] The first cochlear filter implementation using VLSI circuitry was done by Lyon et al[2]. At first the equipment executions of electronic cochlea models utilized simple VLSI as the usage medium because of their little region, fast, and low force utilization. Sarpeshkar actualized the cochlea model as ultra low force programmable simple bionic ear processor [3].Ngamgham et al [4] implemented an eighth order analog filter in state space approach which occupied less area and consumed ultra low power.

The speech processor part is the core of the gadget that models electronically, cochlea of the ear. Numerous such usage utilize the all around acknowledged Patterson's Ear Model, [6] in which models the sound touchy piece of the ear as a bank of sound-related channels and each is liable for a specific band of hearing in the human sound range [5]. The discourse processor comprises of a channel bank to part the discourse range into signs of different data transmissions in the scope of perceptible frequencies. The channel bank possesses the significant segment of the discourse processor which shapes the outside piece of the cochlear embed thus it ought to involve as meager territory as could reasonably be expected. So it becomes basic that an advanced computerized VLSI engineering is to be intended for this application that is customized to meet these necessities [2]. A FPGA usage of the cochlea takes shorter structure time and gave an elite in demolition channel as in Leong et al [7] work. Rekha et al [8] has implemented the cochlea filter on a single FPGA using XSG tool, had good fit to real time data with efficiency of hardware usage. Mahalakshmi et al [9] designed narrow band pass

ISSN: 2250-0839

FIR filters for 16 channels at algorithm level using Kaiser Window with sharp transition band to decompose the audio signals into multiple frequency bands. In this work, investigation is done on the design and hardware implementation of narrow BP FIR filter for speech processor of CI using the XSG tool on FPGA.

II. Speech Processor Techniques

The human hearing system is isolated into four utilitarian units, for instance, a) the outside ear b) the inside ear c) the inner ear and d) the sound-related nerve. The principle helpful unit is the outside ear which involves the pinna and the sound-related channel. The second viable unit is the inside ear which involves three little bones called malleus, incus and stapes. The middle ear goes about as an acoustic impedance matcher and extends the profitability of transmission of sound by lessening the proportion of sound reflection. The third and the most noteworthy valuable unit is the inward ear or the cochlea. The basilar layer in the cochlea is at risk for separating the data signal into different frequencies. The region of inward hair cells along the basilar film chooses the hair cells perfect response to various frequencies. Exactly when sound sign is transmitted through journeying wave in cochlea, the hair cells at the pinnacle respond to low frequencies however hair cells at the base respond to high frequencies as showed up in Figure.1.and analyzed in [10]

TABLE I bandwidth Vs center frequency

Channel number	Center Frequency (Hz)	Frequency range of band pass (3dB-points) Filter (Hz)
1	150	125-175
2	250	225-275
3	350	325-375
4	450	420-480
5	570	530-605
6	700	655-745
7	840	790-890
8	1000	940-1060
9	1170	1105-1235
10	1370	1285-1455
11	1600	1505-1695
12	1850	1745-1955
13	2150	2005-2295
14	2500	2345-2655
15	2900	2705-3095
16	3400	3145-3655

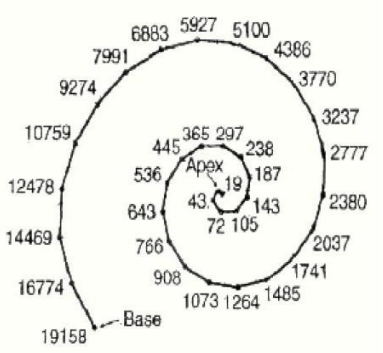

Fig 1 : Speech frequency of basilar membrane

The discourse processor copies the working of the inward ear by separating the discourse signal into 12 to 22 number of recurrence groups so as to remove the sign solidarity to energize the embedded terminal in like manner. Contingent on the discourse handling methodology, the discourse processor extricates different parameters from the acoustic signals and changes over them into electrical signs. The two usually utilized discourse preparing systems are Continuous Interleaved Sampling (CIS) and Advanced Combination Encoder(ACE).Both the speech processing strategy can be realised using filterbank approach and FFT approach

The major manufacturers of CI use the CIS processing strategy. Hence, the work proposed in this study have chosen the filterbank approach of CIS strategy which involves with the functional block diagram as shown in figure.2.

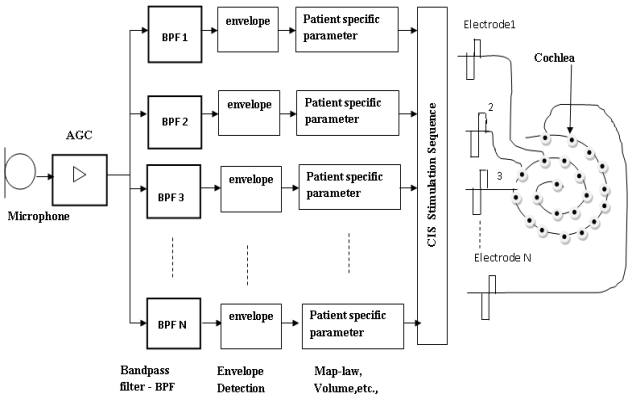

Fig 2 : Functional block diagram of CIS strategy for speech processing

III. FIR Architecture for Speech Processors

A CI is a gadget that can give a feeling of sound to individuals who are hard of hearing or significantly hearing-debilitated. Channels are utilized in numerous parts of audiology and psychoacoustics including the fringe sound-related framework. A channel is a gadget which supports certain frequencies while constricting others. Specifically, a band-pass channel permits a scope of frequencies inside the transfer speed to go through while halting those which are outside the cut-off frequencies. The discourse processor parts the sound-related sign into groups of various frequencies and changes over them into reasonable codes for invigorating the terminals embedded in the cochlea of the ear.

The channel bank approach of CIS is executed here. It comprises of separating the info discourse signals utilizing a computerized band-pass channel bank. Utilizing basic transmission capacity marvel, human discourse recurrence extending from 100 to 3500 Hz, is dispensed to channel groups as in crafted by Rekha et al [3]. This recurrence run is secured by sixteen basic groups, which is appeared in Table I.

The speech processor of the cochlear implant consisting of filter banks, imitates the cochlea of human ear. Design methods for digital filters fall into two broad classes for example, limited motivation reaction (FIR) channel or unbounded drive reaction (IIR) channel. Despite the fact that the attribute of cochlea channel is nonlinear, the direct stage FIR channel is utilized here to beat the burdens of IIR channel because of connection of discourse signal from various channels. FIR has a few favorable circumstances over IIR channels. FIR channels don't have shafts and are unequivocally steady. FIR doesn't amass blunders since they rely upon just a limited number of past information tests. The structure of direct form FIR is shown in Figure 3.

ISSN: 2250-0839

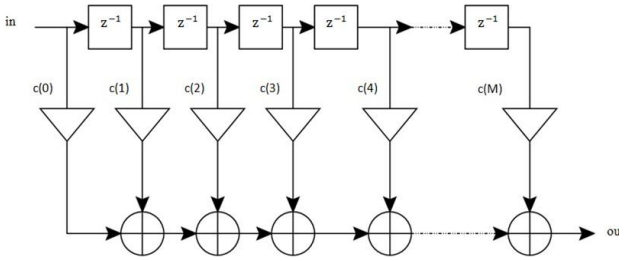

Fig 3: Direct form structure of FIR filter

The speech signal is passed through a bank of band pass filters, which covers the entire speech spectrum range as depicted in Figure 4.

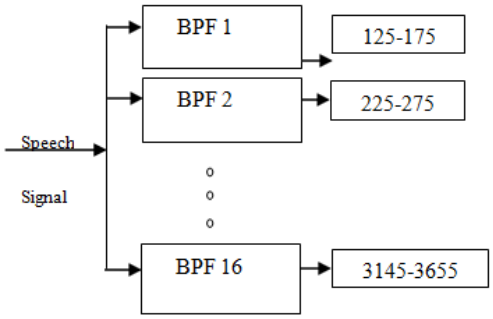

Fig 4: Model of filter bank for speech processor

IV. Proposed Architecture

There is a FIR channel hinder in the System Generator library that utilizes Distributed Arithmetic (DA) to delineate calculation into the FPGA and channel square is eluded as DA FIR. This square gives a profoundly effective parametes, advanced multiplier less engineering for the FIR channel. This work proposes the XSG square level structure for the usage of channel banks utilizing the DA FIR for CI.

DA is an alternate methodology for actualizing advanced channels. The essential thought is to supplant all augmentations and increases by a look into table, barrel shifter and collector as appeared in Figure 5. DA depends on the way that the channel coefficients are known, so increasing c[n]x[n] turns into an augmentation with a steady. This is a significant distinction and an essential for a DA structure.

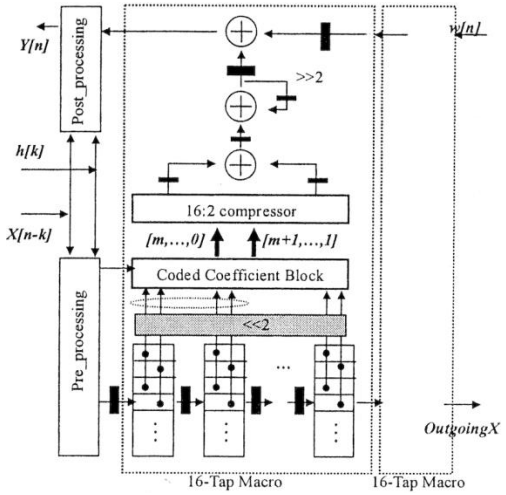

Fig 5: The block diagram for the DA implementation of a FIR filter

Each DA FIR block used in the filter banks requires the coefficients to generate the filter response which is exported from the FDA tool particular to that DA FIR block FDA tool is enabled to generate the required coefficients by providing input parameters like length N of Kaiser window equal to 877, upper cut-off (c2) and lower cut-off (c1) frequencies and β parameter of value equal to 6 in order to obtain stop band attenuation approximately equal to -60dB. The square handling work stream of XSG is utilized in the usage of FIR channel; since it lessens the hour of composing, coding and investigating. The benefit of square handling is that the product itself will change over the preparing square to its equal HDL code. This is called equipment programming co-reproduction and subsequently executing a mind boggling cochlea.

FIR channel is by all accounts simpler by this proposed process. The XSG tool of Xilinx incorporates a FIR Compiler obstruct that speaks to the single FIR BP channel of request 877. The objectives the devoted equipment assets in the FPGA devices with optimized executions. The square outline utilizing XSG block sets for the single FIR BP channel is appeared in Figure 6. Each channel consists of 878 tap DA FIR filter and the corresponding FDA Tool generates 878 numbers of coefficients according to the input parameters provided to produce the magnitude response. The input parameters c1, for each of the 16 channels are obtained from the corresponding critical bands of frequencies

V. Results and Discussions

Input audio signal is fed to the designed DA FIR filter block designed for critical band frequency of 3145 to 3655 Hz as shown in Figure 6 and the input speech spectrum is as shown in Figure 7.

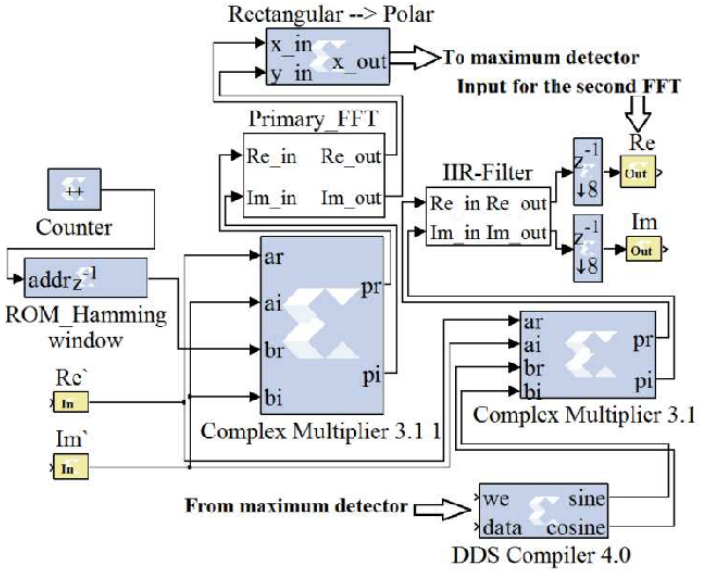

Fig 6: A single DA FIR filter with critical band frequency range of 3145- 3655 Hz

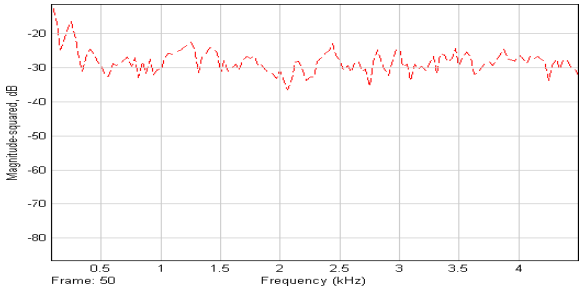

Fig 7: Input speech spectrum for single channel DA FIR filter

ISSN: 2250-0839

Figure 7 shows the filtered output from the single channel of filter bank. In the similar way the other filters in the filterbanks are designed for the sixteen critical bands of frequencies shown in Table I and are implemented using the XSG blocks as shown in the Figure 8. FIR filter in each channel splits the signal into critical bands of frequencies as the basilar membrane in the biological cochlea as shown in figure 9.

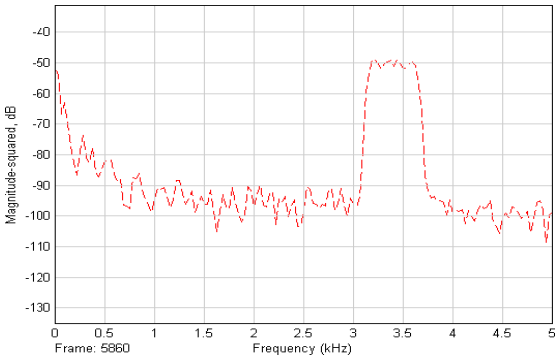

Fig 8: Filtered output for the single channel with critical band frequency of 3145-3655 Hz

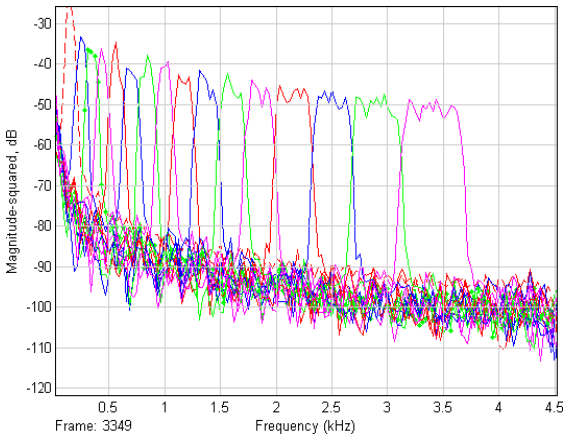

Fig 9: Filtered output from 16 channel filter bank for random source signal

The sixteen channel filter bank implemented by highly parameterized and optimized XSG blocks generates the synthesizable HDL code which is downloaded as the bit stream into FPGA board through Joint Test Association Group (JTAG) cable. XSG block of DA FIR is the software model and JTAG Co-sim is the FPGA hardware model. The synthesizable HDL code generated from the XSG blocks of filter banks is exported to Integrated Sytem Editor (ISE) tool to synthesize and download the designed filter banks on VIRTEX 7 FPGA board.

TABLE II Resource utilization of 16 channel filter bank on Virtex 7 FPGA board

Resources	**Numbers**	**Available on the board**	**% used for implementation**
Slices	43, 804	305,400	14
LUTs	71, 109	74,755	95
Flip flops	71, 109	74,755	95
IOB	65	1200	5

VI. Conclusions

The results of the implemented 16 channel DA FIR based filter bank are validated by experimenting the designed filter bank with real time input speech signal fed through the microphone in the Simulink signal source block as shown in Figure 8 and the corresponding filtered output signal showed the splitting of input speech spectrum to sixteen different critical bands of frequency components. According to CIS algorithm of speech processor the signal energy extracted from the output of these filter banks is converted to stimulating pulse that excites the micro electrodes inside the ear to stimulate the auditory nerve. XSG based DA FIR filter proves that design, analysis and testing of the filter with real time signal is possible in minimal duration of time.

References

[1] Rekha,V.Dundur, M.V.Latte, S.Y.Kulkarni, and M. K.Venkatesha, “Digital Filter for Cochlear Implant Implemented on a Field-Programmable Gate Array”, PWASET, Vol 33, Sep 2008, pp 468-472.

[2] Philipos C. Loizou, “Signal Processing Techniques for Cochlear Implants”, IEEE Engg. in Medicine and Biology, 1999, pp 34- 45.

[3] Hanukumar.V., Seetha Ramaiah.P., “Digital Speech Processing Design for FPGA Architecture for Auditory Prostheses”,Journal of Computer Science And Engineering, Volume 6, Issue 1, March 2011.

[4] S. Rengaprakash et al., "FPGA implementation of fast running FIR filters," 2017 International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET), Chennai, 2017, pp. 1282-1286, doi: 10.1109/WiSPNET.2017.8299970.

[5] M. Slaney, “An Efficient Implementation of the Patterson- Holdsworth Auditory Filter Bank,” Apple Computer Corporate Library, Apple Technical Report #35, 1993.

[6] M. P. Leong, Craig T. Jin and Philip H. W. Leong, “An FPGA- based Electronic Cochlea,” EURASIP Journal on Applied SignalProcessing, no.7, pp.629-638, 2003.

[7] Ngamkham, W., Sawigun, C., Hiseni, S. and Serdijn, W.A. “Analog Complex Gammatone Filter for Cochlear Implant Channels”, Circuits and Systems Proceedings of IEEE International Symposium, pp. 969-972, 2010.

[8] J. Liang and H. K. Kwan, "FIR filter design using multiobjective Cuckoo Search Algorithm," 2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE), Windsor, ON, 2017, pp. 1-4, doi: 10.1109/CCECE.2017.7946828.

[9] Mahalakshmi.P., Reddy.M.R.,“Signal Analysis by using FIR Filter banks in Cochlear Implant Prostheses”, Proceedings of 2010 International Conference on Systems in Medicine and Biology 16-18 December 2010, IIT Kharagpur, India

[10] A. G. Katsiamis, E. M. Drakakis, and R. F. Lyon, “ A Practical Gammatone-Like Filters for Auditory Processing” Hindawi Publishing Corporation, EURASIP Journal on Audio, Speech, and Music Processing, Volume 2007, Article ID 63685, 15 pages,doi:10.1155/2007/63685